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U S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
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INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/03601	October 11, 2000	October 11, 1999

TITLE OF INVENTION
PROCESS AND CIRCUIT ARRANGEMENT FOR DIGITAL FREQUENCY CORRECTION OF A SIGNAL

APPLICANT(S) FOR DO/EO/US Bin YANG, et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☐ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ☒ This is an express request to immediately begin national examination procedures (35 U.S.C. 371(f)).
3. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
4. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
5. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
6. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
7. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
8. ☐ An oath or declaration of the inventor (35 U.S.C. 371(c)(4)).
9. ☐ A translation of the Annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 10-15 below concern document(s) or information included:

10. ☒ An Information Disclosure Statement Under 37 CFR 1.97 and 1.98.
11. ☐ An assignment document for recording.
    Please mail the recorded assignment document to:
    a. ☐ the person whose signature, name & address appears at the bottom of this document.
    b. ☐ the following:
12. ☒ A preliminary amendment.
13. ☒ A substitute specification
14. ☐ A change of power of attorney and/or address letter.
15. ☒ Other items or information:
    Request for International Patent Application Form PCT/RO/101
    International Search Report (Form PCT/ISA/210
    International Publication (WO01/28176)
    PCT/IPEA Forms 416, 409 and 401

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☒ The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees as follows:

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	27 -20=	7	x $ 18.00	126.00
	INDEPENDENT CLAIMS	2 -3=	0	x $ 84.00	0.00
	MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+$280.00	0.00
	BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(4): ☒ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO .....$1,040 ☐ International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO.....$ 890 ☐ International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but international search fee (37 C.F.R. 1.445(a)(2) paid to USPTO...$ 740 ☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provision of PCT Article 33(1)-(4).....$ 710 ☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2) to (4) .....$ 100				1,040.00
	Surcharge of $130 for furnishing the National fee or oath or declaration later than ☐ 20 ☒ 30 mos. from the earliest claimed priority date (37 CFR 1.482(e)).				130.00
			TOTAL OF ABOVE CALCULATIONS		1296.00
	Reduction by 1/2 for filing by small entity, if applicable. Affidavit must be filed also. (Note 37 CFR 1.9, 1.27, 1.28.)				
			SUBTOTAL		1296.00
	Processing fee of $130 for furnishing the English Translation later than [ ] 20 [ ] 30 mos. from the earliest claimed priority date (37 CFR 1.482(f)).				
			TOTAL NATIONAL FEE		1296.00
	Fee for recording the enclosed assignment (37 CFR 1.21(h)).				+
			TOTAL FEES ENCLOSED		1296.00

a. ☒ A check in the amount of $1296.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 19-3935 in the Amount of $ to cover the above fees. A duplicate copy of this sheet is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-3935. A duplicate copy of this sheet is enclosed.

21171
PATENT TRADEMARK OFFICE

SUBMITTED BY: STAAS & HALSEY LLP

Type Name	David M. Pitcher	Reg. No.	25,908
Signature	David M. Pitcher	Date	April 4, 2002

Docket No.: 1516.1002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of 35 U.S.C. §371 OF:

Bin YANG, et al.

Based Upon International Serial No. PCT/DE00/03601

Group Art Unit: To Be Assigned

Confirmation No.

U.S. Filing Date:

Examiner: To Be Assigned

For: PROCESS AND CIRCUIT ARRANGEMENT FOR DIGITAL FREQUENCY CORRECTION OF A SIGNAL

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Before examination of the above-identified application, please amend the application as follows:

IN THE ABSTRACT:

Please REPLACE the originally filed Abstract with the enclosed unmarked Substitute Abstract.

IN THE SPECIFICATION:

Please REPLACE the originally filed Specification with the enclosed unmarked Substitute Specification.

IN THE CLAIMS:

Please REPLACE claims 1-17 and ADD new claims 18-27 in accordance with the following:

1. (ONCE AMENDED) A method of a digital frequency correction, comprising:

sampling a signal with a sampling cycle (k) and digitalized (x(k));

processing an N-step CORDIC algorithm so that a frequency of a signal (x(k)) is altered

at a predetermined frequency;

representing the signal (x(k)) a first vector comprising a first in-phase component (i_0) and a first quadrature component (q_0) in a complex I/Q plane;

imaging the first vector by applying the CORDIC algorithm onto a second vector with a second in-phase component (I_n) and a second quadrature component (Q_N), wherein the second vector represents a signal with an altered frequency and phase; and

composing a predetermined angle (z(k)) of N different rotation angles (α_n), wherein each of the different rotation angles (α_n) are calculated according to $\arctan(2^{-n})$, n = 0, 1,..., N-1, and are respectively provided with a sign (σ_n) providing a direction of rotation.

2. (ONCE AMENDED) The method as recited in claim 1, wherein the predetermined angle (z(k)) is limited to a range of 0 to 2π, and where the predetermined angle (z(k)) is represented by a register value (w(k)), a bit width N_w prescribing the range of 0 to 2π for the predetermined angle (z(k)), a register value (w(k)) being calculated in each cycle (k) of the sampling cycle by an addition of a value (f· T/m), allocated to the predetermined angle (z(k)), and a register value w(k-1)) of the preceding cycle (k-1) of the sampling cycle, where an overflow of the register value (w(k)) is neglected.

3. (ONCE AMENDED) The method as recited in claim 2, wherein the predetermined angle (z(k)) is limited to a range of $-\pi/2$ to $+\pi/2$, where a quadrant correction is carried out before the CORDIC algorithm, and the first in-phase component (i_0) and the first quadrature component (q_0) are respectively multiplied by $(-1)^2$, s = 0, 1.

4. (ONCE AMENDED) The method as recited in claim 3, wherein the bit width N_w of the register value (w(k)) comprises:

$$N_w \geq \log2(m) - \log2(\Delta f \cdot T),$$

where m comprises an oversampling factor of the signal (x(k)) and T represents a duration of a digital value of the signal (x(k)).

5. (ONCE AMENDED) The method as recited in claim 4, wherein a number N of operations of the CORDIC algorithm for a predetermined signal to phase noise ratio SNR and the bit width N_w of the register value (w(k)) comprises a following condition:

$(SNR + 3)/6 \leq N \leq N_w - 2.$

6. (ONCE AMENDED) The method as recited in claim 5, wherein two guard bits are provided in each operation of the CORDIC algorithm, and an input and output bit width of the CORDIC algorithm is at least greater than N + 2.

7. (ONCE AMENDED) An apparatus of a digital frequency correction of a signal, which is sampled with a sample cycle (k) and is digitized (x(k)), comprising:

N micro-rotation blocks receiving a signal (i_0, q_0);

a sign table providing to each micro-rotation block a sign (σ_n) from a sign table,];

a register driving the sign table and supplying a register value (w(k));

a delay element; and

an adder adds] adding a predetermined frequency value (f•T/m) to an output value of the delay element, outputting a result indicative thereof, and storing the result in the register, wherein the register value of a preceding cycle (k-1) is supplied to the delay element.

8. (ONCE AMENDED) The apparatus as recited in claim 7, further comprising:

a quadrant correction block preceding the micro-rotation blocks, to which an input signal (s) is supplied, rotating the signal into a first or fourth quadrant of the complex I/Q plane and providing a vector (i_0, q_0) representing the signal being rotated.

9. (ONCE AMENDED) The apparatus as recited in claim 8, wherein each micro-rotation block comprises:

two shift registers shifting components of an input vector (I_n, Q_n) of the micro-rotation block by n bits and providing output values, and

two accumulators adding the components of the input vector (I_n, Q_n) to the output values of the shift registers, the output values of the shift registers being provided with the sign (σ_n) allocated to the respective micro-rotation block.

10. (ONCE AMENDED) The apparatus as recited in claim 9, wherein the sign table comprises a read-only memory comprising 2^N (N - 2) bits, an XOR gate, and an inverter to produce a sign (σ_0, σ_1) for the first and second micro-rotation blocks and the input signal (s) for the quadrant correction block.

11. (ONCE AMENDED) The apparatus as recited in claim 10, wherein the input signal (s) for the quadrant correction block is formed by a logical XOR operation on two lowest-value bits (w_0, w_1) of the register value (w(k)).

12. (ONCE AMENDED) The apparatus as recited in claim 11, wherein the sign (σ_0) for the first micro-rotation block corresponds to a second bit (w_1) of the register value (w(k)).

13. (ONCE AMENDED) The apparatus as recited in claim 12, wherein the sign (σ_1) for the second micro-rotation block corresponds to an inverted third bit (w_2) of the register value (w(k)).

14. (ONCE AMENDED) The apparatus as recited in claim 13, the apparatus further comprising:

a receiver of a mobile radio device, comprising:

a baseband filter with stages filtering and processing a received baseband signal (x(k)); and

a last stage of the baseband filter to correct the frequency of the baseband signal x(k)).

15. (ONCE AMENDED) The apparatus as recited in claim 14, further comprising:

an offset compensation of the baseband signal (x(k)) to remove DC portions.

16. (ONCE AMENDED) The apparatus as recited in claim 14, wherein a GSM or UMTS mobile radio device comprises the receiver.

17. (ONCE AMENDED) The apparatus as recited in claim 15, wherein the apparatus provides a communication system for digital IF mixing and/or frequency correction.

18. (NEW) The method as recited in claim 1, wherein the predetermined angle (z(k)) is limited to a range of $-\pi/2$ to $+\pi/2$, where a quadrant correction is carried out before the CORDIC algorithm, and the first in-phase component (i_0) and the first quadrature component (q_0) are respectively multiplied by $(-1)^2$, s = 0, 1.

19. (NEW) The method as recited in claim 2, wherein the bit width N_w of the register value (w(k)) comprises:

$$N_w \geq \log2(m) - \log2(\Delta f \cdot T),$$

where m comprises an oversampling factor of the signal (x(k)) and T represents a duration of a digital value of the signal (x(k)).

20. (NEW) The method as recited in claim 18, wherein a number N of operations of the CORDIC algorithm for a predetermined signal to phase noise ratio SNR and the bit width N_w of the register value (w(k)) comprises a following condition:

$$(SNR + 3)/6 \leq N \leq N_w - 2.$$

21. (NEW) The method as recited in claim 2, wherein a number N of operations of the CORDIC algorithm for a predetermined signal to phase noise ratio SNR and the bit width N_w of the register value (w(k)) comprises a following condition:

$$(SNR + 3)/6 \leq N \leq N_w - 2.$$

22. (NEW) The apparatus as recited in claim 7, wherein each micro-rotation block comprises:

two shift registers shifting components of an input vector (I_n, Q_n) of the micro-rotation block by n bits and providing output values, and

two accumulators adding the components of the input vector (I_n, Q_n) to the output values of the shift registers, the output values of the shift registers being provided with the sign (σ_n) allocated to the respective micro-rotation block.

23. (NEW) The apparatus as recited in claim 8, wherein the sign table comprises a read-only memory comprising 2^N (N - 2) bits, an XOR gate, and an inverter to produce a sign (σ_0, σ_1) for the first and second micro-rotation blocks and the input signal (s) for the quadrant correction block.

24. (NEW) The apparatus as recited in claim 10, wherein the sign (σ_0) for the first micro-rotation block corresponds to a second bit (w_1) of the register value (w(k)).

25. (NEW) The apparatus as recited in claim 10, wherein the sign (σ_1) for the second

micro-rotation block corresponds to an inverted third bit (w_2) of the register value (w(k)).

26. (NEW) The apparatus as recited in claim 11, wherein the sign (σ_1) for the second micro-rotation block corresponds to an inverted third bit (w_2) of the register value (w(k)).

27. (NEW) The apparatus as recited in claim 15, wherein a GSM or UMTS mobile radio device comprises the receiver.

REMARKS

This Preliminary Amendment is submitted to improve the form of the specification as originally-filed. It is respectfully requested that this Preliminary Amendment be entered in the above-referenced application.

In accordance with the foregoing, claims 1-17 have been amended and claims 18-27 have been added. Claims 1-27 are pending and are under consideration.

If there are any questions regarding these matters, such questions can be addressed by telephone to the undersigned. Otherwise, an early action on the merits is respectfully solicited.

If any further fees are required in connection with the filing of this Preliminary Amendment, please charge same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: April 4, 2002

By: David M. Pitcher

David M. Pitcher
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Serial No.: To Be Assigned
Docket No.: 1516.1002

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT:

Please REPLACE the originally filed Abstract with the enclosed marked-up Substitute Abstract.

IN THE SPECIFICATION:

Please REPLACE the originally filed Specification with the enclosed marked-up Substitute Specification.

IN THE CLAIMS:

Please AMEND claims 1-17 in accordance with the following:

1. (ONCE AMENDED) A method of [Process for the] a digital frequency correction, comprising:

sampling [of] a signal [, which is sampled] with a sampling cycle (k) and digitalized (x(k)) [and which is processed by means of,];

processing an N-step CORDIC algorithm so that [the] a frequency of [the] a signal (x(k)) is altered [by] at a [predeterminable] predetermined frequency[, wherein];

representing the signal (x(k)) [is represented by] a first vector [with the] comprising a first in-phase component (i_0) and [the] a first quadrature component (q_0) in [the] a complex I/Q plane[,];

[wherein] imaging the first vector [is imaged by means of] by applying the CORDIC algorithm onto a second vector with a second in-phase component (I_n) and a second quadrature component (Q_N), [and] wherein the second vector represents [the] a signal with an altered frequency and phase[,]; and

[wherein] composing a [the] predetermined angle (z(k)) [is composed of a plurality] of N different rotation angles (α_n), wherein each of the different rotation angles (α_n) are calculated according to [the formula] $\arctan(2^{-n})$, n = 0, 1, ..., N-1, and are respectively provided with a sign (σ_n) [which gives the] providing a direction of rotation.

2. (ONCE AMENDED) [Process according to] The method as recited in claim 1, [in which] wherein the predetermined angle (z(k)) is limited to a range of 0 to 2π, and where [in that]

the predetermined angle (z(k)) is represented by a register value (w(k)), [the] a bit width N_w [of which prescribes] prescribing the range of 0 to[-]2π for the predetermined angle (z(k)), [the] a register value (w(k)) being calculated in each cycle (k) of the sampling cycle by [the] an addition of a value $(f \cdot T/m)$, allocated to the predetermined angle (z(k)), and [of the] a register value w(k-1)) of the preceding cycle (k-1) of the sampling cycle, [and] where an overflow of the register value (w(k)) is neglected.

3. (ONCE AMENDED) [Process according to] The method as recited in claim [1 or] 2, wherein the predetermined angle (z(k)) is limited to a range of $-\pi/2$ to $+\pi/2$, [in that] where a quadrant correction is carried out before the CORDIC algorithm, [whereby] and the first in-phase component [(i_n)] (i_0) and the first quadrature component (q_0) are respectively multiplied by $(-1)^2$, s = 0, 1.

4. (ONCE AMENDED) [Process according to one of the foregoing claims] The method as recited in claim 3, wherein the bit width N_w of the register value (w(k)) [fulfills the following] comprises:

$$N_w \geq \log2(m) - \log2(\Delta f \cdot T),$$

where m [represents] comprises an [the] oversampling factor of the signal (x(k)) and T represents [the symbol] a duration of a digital value of the signal (x(k)).

5. (ONCE AMENDED) [Process according to one of claims 2-4] The method as recited in claim 4, wherein [the] a number N of [the steps] operations of the CORDIC algorithm for a predetermined signal to phase noise ratio SNR and [a] the bit width N_w of the register value (w(k)) [fulfills the] comprises a following condition:

$$(SNR + 3)/6 \leq N \leq N_w - 2.$$

6. (ONCE AMENDED) [Process according to one of the foregoing claims] The method as recited in claim 5, wherein two guard bits are provided in each [step] operation of the CORDIC algorithm, and [the] an input and output bit width of the CORDIC algorithm is at least greater than N + 2.

7. (ONCE AMENDED) An apparatus of [Device for the] a digital frequency

correction of a signal, which is sampled with a sample cycle (k) and is digitized (x(k)), comprising:

[in which a series circuit of] N micro-rotation blocks [(11-13) is provided, to which the] receiving a signal (i_0, q_0) [is supplied,];

a sign table providing to each micro-rotation block a sign (σ_n) [is supplied to each micro-rotation block [(11-13)] from a sign table [(14)],];

a register [(31) is provided,] driving the sign table and supplying a [the] register value (w(k)) [of which is supplied as an address to the sign table (14),];

a delay element; and

an adder [(18) and a delay element (19) are provided, and the adder [(18)] adds] adding a predetermined frequency value (f•T/m) to [the] an output value of the delay element [(19)], outputting a result indicative thereof, and [stores the] storing the result in the register [(31)], [and] wherein the register value of [the] a preceding cycle (k-1) is supplied to the delay element [(19)].

8. (ONCE AMENDED) [Device according to] The apparatus as recited in claim 7, [wherein] further comprising:

a quadrant correction block preceding the [series circuit of the] micro-rotation blocks [(11-13) is preceded by a quadrant correction block (10)], to which an input signal (s) is supplied, rotating the signal [a vector (i_0, q_0) representing the signal being rotated] into [the] a first or fourth quadrant of the complex I/Q plane [by means of the quadrant correction block (10)] and providing a vector (i_0, q_0) representing the signal being rotated.

9. (ONCE AMENDED) [Device according to claim 7 or 8] The apparatus as recited in claim 8, wherein each micro-rotation block [(11-13) has] comprises:

two shift registers [(20, 21) for] shifting [the] components of an input vector (I_n, Q_n) of the micro-rotation block [(11-13)] by n bits and providing output values, and

two accumulators [(22, 23) for] adding the components of the input vector (I_n, Q_n) to the output values of the shift registers [(20, 21)], the output values of the shift registers [(20, 21)] being provided with the sign (σ_n) allocated to the respective micro-rotation block [(11-13)].

10. (ONCE AMENDED) [Device according to claim 7, 8 or 9] The apparatus as recited in claim 9, wherein the sign table [(14) has] comprises a read-only memory [for] comprising 2^N (N - 2) bits, [and] an XOR gate [(16)], and an inverter [(17) for the production of] to

produce [the] a sign (σ_0, σ_1) for the first and second micro-rotation blocks [(11, 12)] and the input signal (s) for the quadrant correction block [(10)].

11. (ONCE AMENDED) [Device according to claim 10] The apparatus as recited in claim 10, wherein the input signal (s) for the quadrant correction block [(10)] is formed by a logical XOR operation on [the] two lowest-value bits (w_0, w_1) of the register value (w(k)).

12. (ONCE AMENDED) [Device according to claim 10 or 11] The apparatus as recited in claim 11, wherein the sign (σ_0) for the first micro-rotation block [(11)] corresponds to [the] a second bit (w_1) of the register value (w(k)).

13. (ONCE AMENDED) [Device according to claim 10, 11 or 12] The apparatus as recited in claim 12, wherein the sign (σ_1) for the second micro-rotation block [(12)] corresponds to [the] an inverted third bit (w_2) of the register value (w(k)).

14. (ONCE AMENDED) [Receiver] The apparatus as recited in claim 13, the apparatus further comprising:

a receiver of a mobile radio device, comprising: [which has]

a baseband filter with [plural] stages [(24-30) for] filtering and processing a received baseband signal (x(k))[, and in which the process according to one of claims 1-6 and/or the device according to one of claims 7-13 is provided before the]; and

a last stage [(28)] of the baseband filter [for] to correct the frequency [correction] of the baseband signal x(k)).

15. (ONCE AMENDED) Receiver according to] The apparatus as recited in claim 14, further comprising: [wherein]

an offset compensation [(26)] of the baseband signal (x(k)) [is provided for removing] to remove DC portions[, before the process according to one of claims 1-6 and/or the device according to one of claims 7-13].

16. (ONCE AMENDED) [Receiver according to claim 14 or 15] The apparatus as recited in claim 14, wherein [the receiver is used in] a GSM or UMTS mobile radio device comprises the receiver.

17. (ONCE AMENDED) The apparatus as recited in claim 15, wherein the apparatus provides [Use of the process according to one of claims 1-6 and/or of the device according to one of claims 7-13 in] a communication system for digital IF mixing and/or frequency correction.

SUBSITUTE SPECIFICATION

TITLE OF THE INVENTION

PROCESS AND CIRCUIT ARRANGEMENT FOR DIGITAL FREQUENCY CORRECTION OF A SIGNAL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of and priority to International Application PCT/DE00/03601, filed October 11, and German Patent Application GR 99 P 5026, filed October 11, 1999, the contents of each of which are incorporated herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The invention relates to a process and a circuit arrangement for digital frequency correction of a signal, in particular for use in a transceiver circuit, by sampling the signal with a predetermined cycle and processed using an N-step CORDIC algorithm so that a frequency of the signal is altered by a predetermined frequency.

2. Description of the Related Art

[0003] In transceiver circuits, local oscillators are used to produce a reference frequency. Particularly because of production tolerances, temperature fluctuations, and supply voltage fluctuations, undesired fluctuations of the reference frequency can occur. The undersigned fluctuations of the reference frequency causes a signal to be processed having large frequency fluctuations, and a power of the transceiver circuit is thereby reduced.

[0004] In order to counteract the undesired fluctuations, expensive and high quality oscillators are, for example, used in the transceiver circuits, to produce a very stable reference frequency, i.e., an oscillator which is precise and free from fluctuation. Likewise, oscillators compensated for voltage fluctuations and for temperature variations can also be used to reduce a dependence on the reference frequency for the voltage fluctuations and the temperature variations. Furthermore, so-called automatic frequency correction control loops (AFC loops) are frequently used to precisely set the local reference frequency. However, the AFC loops are disadvantageous in that the AFC loops are expensive and very costly in circuit technology.

[0005] In order to keep the costs of the transceiver low, in particular for use in mass produced articles, such as mobile telephones, cheap oscillators have been used which have neither a voltage supply control device nor a temperature control device. However, particularly in such products, no excessive fluctuation of the reference frequency can be tolerated. A subsequent correction of the frequency of the signal to be processed is therefore unconditionally necessary.

[0006] A frequency correction process of a baseband signal x in a transceiver circuit, for example of a mobile radio receiver, can be represented mathematically as follows: sampling values x(k) of the baseband signal x(k) = i(k) + j·q(k) (with j = sqrt(-1)), symbols which have a symbol duration T, are multiplied by sampling values of a (complex) frequency correction signal z(k) = 2πt·T/m·k, m being an oversampling factor. The multiplication in a time domain corresponds in a frequency domain to a frequency displacement of the baseband signal x(k) by a frequency f. In a complex signal pointer plane, the multiplication represents a rotation of the "pointer" x(k) through an angle z(k):

$$x(k)\exp(j\,z(k)) = [i(k) + j\cdot q(k)][\cos(z(k)) + j\sin(z(k))]$$
$$= [i(k)\cos(z(k)) - q(k)\sin(z(k))] + j\,[i(k)\sin(z(k)) + q(k)\cos(z(k))]$$

[0007] The more precise and more finely adjustable a frequency correction signal z(k), the better the frequency correction; i.e., the "pointer" x(k) can be rotated in finer steps in the complex plane.

[0008] The frequency correction according to the above equation may be calculated using digital multipliers and coefficient tables for a sine and cosine functions; which demands, though, a very high circuit technology cost which makes such a solution expensive and costly. In particular, when embodied as an integrated circuit, this solution requires a large chip surface and is, therefore, very expensive.

SUMMARY OF THE INVENTION

[0009] The invention therefore has as its object to provide a process and a circuit arrangement for digital frequency correction, particularly for use in a transceiver circuit, which produces a very precise frequency correction with a small circuit technology cost.

[0010] The above and other objects are attained using a process.

[0011] An exemplary embodiment of the present invention includes an CORDIC (Coordinate Rotation Digital Computer) algorithm for digital frequency correction of a signal. Namely, a frequency and phase correction can be carried out relatively simply using the CORDIC algorithm. The CORDIC algorithm can be carried out with a small circuit technical cost, so that costs of a circuit based on the CORDIC algorithm and an inexpensive oscillator are smaller than the costs of a compensated oscillator.

[0012] The CORDIC algorithm is described in J.E. Volder, "The CORDIC trigonometric computing technique", IRE Trans. Electronic Computers, Vol.8, pp. 340-344, 1959, This algorithm is n-fold iterative and serves to rotate a vector through a defined angle $\alpha_n = \arctan(2^{-n})$, n = 0, 1,..., N-1. If the vector represents a pointer of a complex signal, a change in a frequency of the signal corresponding to a multiplication by a frequency correction signal is possible by means of this rotation. The rotation angle becomes smaller with each iteration ($\alpha_0 = 45° > \alpha_1 = 26.6° > \ldots > \alpha_{N-1}$, so that the frequency of the signal changes in smaller steps with increasing iteration steps.

[0013] The iterative rotation through an angle a can be represented by the following linear combination:

$$a = \sigma_0\alpha_0 + \sigma_1\alpha_1 + \ldots + \sigma_{N-1}\alpha_{N-1} \quad (\sigma_n = \pm 1)$$

[0014] A precision of the rotation is predetermined by the smallest rotation angle α_{N-1}. A direction of rotation (+1 counterclockwise, -1 clockwise) is given by the sign σ_n.

[0015] A signal which is represented by sampling values of the in-phase component I_n and the quadrature component Q_n is iteratively rotated through the angle a by the CORDIC algorithm. For this purpose, the individual rotations according to the CORDIC algorithm can be executed by simple shift and addition operations:

$$I_{n+1} = I_n - \sigma_n 2^{-n} Q_n$$

$$Q_{n+1} = \sigma_n 2^{-n} I_n + Q_n$$

[0016] The above equation can also be represented as follows, using the equation $\alpha_n = \arctan(2^{-n})$ for the rotation angle:

$$I_{n+1} = \mathrm{sqrt}(1 + 2^{-2n}) \left[\cos(\sigma_n \alpha_n)\, I_n - \sin(\sigma_n \alpha_n)\, Q_n\right]$$

$$Q_{n+1} = \text{sqrt}(1 + 2^{-2n}) \, [\sin(\sigma_n \alpha_n) \, I_n + \cos(\sigma_n \alpha_n) \, Q_n]$$

[0017] After N rotations, the following is obtained:

$$I_N = K \, [\cos(z) \, I_0 - \sin(z) \, Q_0]$$

$$Q_N = K \, [\sin(z) \, I_0 + \cos(z) \, Q_0]$$

with K = 1.647. The signal to be corrected can be adjusted in frequency using the process described above.

[0018] In the process according to the invention, the complex multiplication of the sample values x(k) of the signal, particularly of a baseband signal, by the frequency correction signal z(k) is now executed using the CORDIC algorithm. Because a principle no "rigid" frequency correction occurs, and a frequency correction which is variable because of the CORDIC algorithm, the constancy of a reference signal of the oscillator does not play a significant part.

[0019] In order to use the CORDIC algorithm for the process according to the present invention, a few disadvantages of the CORDIC algorithm must however be compensated for by the invention. In particular, because the CORDIC algorithm allows only a limited correction range of a rotation angle of approximately 99°, a reduction of the rotation angle required for correction is required. It is provided, according to the invention, for this purpose to correct the rotation angle so that the rotation angle always has a value less than or equal to 90°. The rotation angle represented by z(k) is a stored modulo 2π in a register of a bit width N_w. The value w(k) stored in the register is accumulated according to an equation w(k) = w(k-1) + f•T/m. A value 111...111 for w(k) corresponds to a greatest value $1 - 2^{N}_{w}$, corresponding to an angle of $2\pi \, (1 - 2^{N}_{w})$. The modulo 2π operation is, thus, attained by simply neglecting an overflow of the register.

[0020] Furthermore, in order to provide optimum execution of the CORDIC algorithm, the pointer z(k) needs to be represented by a frequency correction signal lying in a first or a fourth quadrant of a complex I/Q plane. For this purpose, an in-phase and quadrature components of the pointer of the signal to be corrected are respectively multiplied by $(-1)^s$, s = 0.1, in order to turn the pointer through the angle $z(k) - \pi$ when the pointer lies in a second or a third quadrant of the complex I/Q plane.

[0021] A sign flag s is calculated like the sign σ_n for the individual iterations (micro-rotations) of the CORDIC algorithm. According to the invention, a sign table is provided for this purpose, in which the corresponding sign of the micro-rotation is set out for all possible micro-rotations, such that the sign flag s and the two signs σ_0 and σ_1 are calculated directly and the remaining signs σ_n, n = 2, 3,..., N-1 are calculated from the bits w_1, w_2, w_3,..., w_{N+1} of a value w(k) stored in the register.

[0022] The bit width N_w of the register and the number of micro-rotations N of the CORDIC algorithm affect the correction range or a phase noise of the frequency-corrected signal x(k) exp(jz(k)) and are therefore to be chosen according to the present invention as follows. A bit width N_w is to fulfill the following inequality for a correctable frequency range Δf:

$$N_w \geq \log2(m) - \log2(\Delta f \cdot T)$$

[0023] For a desired signal to phase noise ratio SNR, a number N of the micro-rotations is chosen as follows:

$$(SNR + 3)/6 \leq N \leq N_w - 2$$

[0024] The desired signal to phase noise ratio SNR is thus attained, an upper limit for N being predetermined by the bit width of the register.

[0025] Finally, another two guard bits have to be provided in each iteration of the algorithm during the implementation of the CORDIC algorithm, in order to be able to process the greatest possible value of the scaling factor, namely sqrt(2) K = sqrt(2) 1.647 2.33. K is a scaling factor because of the CORDIC algorithm and sqrt(2) is a possible "growth factor" of the in-phase and quadrature components due to the CORDIC algorithm. Accordingly, an input bit width and an output bit width of the CORDIC algorithm should be as great as possible, for instance, at least greater than N + 2. A greater phase noise would otherwise be produced by rounding errors of the CORDIC algorithm than by phase errors.

[0026] These together with other objects and advantages, which will be subsequently apparent, reside in the details of construction and operation as more fully hereinafter described and claimed, reference being had to the accompanying drawings forming a part hereof, wherein like numerals refer to like parts throughout.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The following description of preferred embodiments of the invention, using the accompanying drawings, serves for further explanation of the invention.

FIG. 1 shows a block circuit diagram with essential components for carrying out a process according to the invention,

FIG. 2 shows a structure of a sign table for a CORDIC algorithm,

FIG. 3 shows a structure of a micro-rotation block for a CORDIC algorithm, and

FIG. 4 shows a use of the process, according to the invention, in a transceiver of a GSM mobile telephone.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] In FIG. 1, sampling values i_0 and q_0 of an in-phase or quadrature components of a complex baseband signal x(k) are supplied to a quadrant correction block 10, where k denotes discrete sampling times. The quadrant correction block 10 causes a pointer represented by the baseband signal x(k) to lie in a first or fourth quadrant of a complex in-phase/quadrature I/Q plane. Namely, if the pointer lies in a second or third quadrant, CORDIC algorithm does not work correctly. As already described, the in-phase and quadrature components have to be respectively multiplied by -1 if the pointer is situated in the second or third quadrant of the complex I/Q plane.

[0029] N micro-rotation blocks in sequence follow the quadrant correction block 10 although three of these blocks, 11, 12, 13, are shown, a one of ordinary will appreciate that more blocks may be implemented. Each micro-rotation block calculates a step of the CORDIC algorithm, i.e., rotates the pointer represented by the in-phase and quadrature components in the complex I/Q plane through an angle $\pm \alpha_n = \pm \arctan(2^{-n})$. Components I_0 and Q_0 are present at an input of a micro-rotation block 11, and represent at an output, as the components I_1 and Q_1, a pointer rotated through the angle $\pm \alpha_0 = \pm \arctan(1)$. The components I_2 and Q_2 are present at an output of a micro-rotation block 12, and represent a pointer rotated through an angle $\pm \alpha_1 = \pm \arctan((2^{-1}))$. Finally, a pointer represented by in-phase component I_n and an original quadrature Q_n and representing the frequency-corrected complex baseband signal is present at an output of a micro-rotation block 13 after passage through N steps of the CORDIC algorithm. The rotation is either counterclockwise or clockwise in each rotation in a micro-rotation block.

The direction of rotation depends on a sign σ_n.

[0030] The sign σ_n and an input signal s for the quadrant correction block 10 are produced by a sign table 14. The sign table 14 is driven by a register 31 with a bit width N_w in which a register value w with N_w bits is deposited. The first (N+2) bits of w(k) of a register 31 are supplied to the sign table 14.

[0031] The structure of the sign table 14 is shown in FIG. 2. The input signal s for the quadrant block 10 is calculated by a logical XOR operation 16 on two lowest bits w_0 and w_1 of the register value w. A first sign σ_0 corresponds directly to the bit w_1 of the register value w. A second sign σ_1 is calculated by inverting 17 a bit w_2 of the register value w. Remaining signs σ_2 through σ_{N-1} are deposited in a read-only memory 15 (ROM), in which 2^N (N-2) bits are stored. The ROM or read-only memory 15 can be made smaller by a calculation of s, σ_0 and σ_1 from the three lowest bits w_0-w_2; namely, a memory capacity of 2^{N+2} (N + 1) bits would otherwise be required.

[0032] The following table clarifies the calculation of s, σ_0 and σ_1 from the three lowest bits w_0 through w_2 of the register value w, and a corresponding rotation angle range:

w_0	w_1	w_2	Rotation angle range		Quadrant	s	σ_0	σ_1
0	0	0	0°	45°	I	0	0	1
0	0	1	45°	90°	I	0	0	0
0	1	0	90°	135°	II	1	1	1
0	1	1	135°	180°	II	1	1	0
1	0	0	180°	225°	III	1	0	1
1	0	1	225°	270°	III	1	0	0
1	1	0	270°	315°	IV	0	1	1
1	1	1	315°	360°	IV	0	1	0

[0033] The signs σ_n are coded such that a logical "0" means a counter-clockwise rotation and a logical "1" means a clockwise rotation. Input bits of the sign table 14, i.e., of the register value w, are calculated cumulatively, w(k) = w(k-1) + f•T/m, starting from the default value f•T/m. An adder 18 and a delay element 19 are provided for this purpose. The delay element 19 delays the last register value w(k-1) by the time T/m. The adder 18 then adds the default value f•T/m, which predetermines a correction frequency f, to w(k-1). A result of the addition then gives a new register value for the register 31.

[0034] The structure of a micro-rotation block, which calculates the basic CORDIC operation previously described,

$$I_{n+1} = I_n - \sigma_n 2^{-n} Q_n$$

$$Q_{n+1} = \sigma_n 2^{-n} I_n + Q_n$$

is shown in FIG. 3. For this purpose, a first and a second shift register, 20 or 21 respectively, are provided, respectively shifting the in-phase component I_n or the original quadrature component Q_n by n bits (2^{-n}). The in-phase component or the original quadrature component shifted by n bits is then multiplied by the sign σ_n or $-\sigma_n$, i.e., the sign of the displaced component is correspondingly altered, and is added to the original quadrature component Q_n or in-phase component I_n in a first 22 or second 23 accumulator, respectively. The result is a rotated pointer, represented by the in-phase component I_{n+1} and the quadrature component Q_{n+1}.

[0035] FIG. 4 shows an exemplary use of the process according to the present invention in a transceiver of a GSM mobile telephone. Sampling values x(k) of a baseband signal are supplied to a digital prefilter 24 which is operated with a high cycle rate, which is a multiple of a sampling rate of 2 of the baseband signal.

[0036] Following the digital prefilter 24 is a first decimator 25, which divides the high cycle rate of the output signal of the prefilter 24 into a lower cycle rate. The first decimator 25 is provided with an offset compensation block 26 for the compensation of a DC offset, i.e., a DC portion, possibly contained in the baseband signal. The DC offset to be compensated is predetermined for the offset compensation block 26 by a digital signal processor 30. The digital signal processor 30, based on first sampling values of the baseband signal, estimates an offset or DC portion possibly contained in the baseband signal, and supplies the estimated offset or DC portion to the offset compensation block 26 for compensation. If the offset or the DC portion of the baseband signal is removed, the offset would be transformed by the CORDIC algorithm into an interfering sine signal, which for example, is only to be expensively removed again in the digital signal processor 30.

[0037] The offset compensation block 26 is followed by a CORDIC frequency correction block 27 for carrying out the process according to the present invention. The correction frequency f by which the baseband signal is to be corrected is supplied to the CORDIC frequency correction block 27 by the digital signal processor 30. The CORDIC frequency

correction block 27 corrects the baseband signal frequency, as previously described, by the correction frequency f.

[0038] The CORDIC frequency correction block 27 is followed by a digital postfilter 28, which is cycled at precisely twice the sampling rate 2 of the baseband signal. The digital postfilter 28 is a low pass filter with a large edge steepness and serves to remove interfering frequencies and noise of the baseband signal.

[0039] The frequency-corrected and many times filtered baseband signal is then decimated by a second decimator 29 by a factor 2 to the sampling rate of the baseband signal, and is supplied to the digital signal processor 30 for further processing.

[0040] The process according to the present invention and the corresponding device for carrying out the process may also be used for frequency correction in a transmitter and a receiver of a UMTS (Universal Mobile Telecommunication System) mobile radio device. A further application is a use of the process according to the present invention everywhere in transmitters and receivers where the process according to the invention and the corresponding device serves, in addition to frequency correction, also for digital frequency mixing. Because the functions of frequency correction and frequency mixing are very often used, traditional mixers can be saved in this manner and thus the cost can again be markedly reduced. Examples of such a transmitter and receiver are found in cordless telephones of the DECT standard (Digital Enhanced Cordless Telephone), DVB (Digital Video Broadcasting), and cable modems.

[0041] Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

ABSTRACT OF DISCLOSURE

A method and a circuit for the digital correction of a frequency of a signal, especially for use in a transmitter/receiver circuit include rotating a signal "pointer" (i0, q0) using a CORDIC algorithm, through a predetermined angle in a complex I/Q plane corresponding to a correction frequency. The CORDIC algorithm includes micro-rotation blocks corresponding to N stages, and a character table and a register.

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Process and circuit arrangement for digital frequency correction of a signal

The invention relates to a process and a circuit arrangement for digital frequency correction of a signal, in particular for use in a transceiver circuit, according to the preamble of claim 1 or 7.

In transceiver circuits, local oscillators are used for producing a reference frequency. Particularly because of production tolerances, temperature fluctuations, and supply voltage fluctuations, undesired fluctuations of the reference frequency can occur. This causes the signal to be processed likewise to have large frequency fluctuations, and the power of the transceiver circuit is thereby reduced.

In order to counteract this, expensive and high quality oscillators are for example used in the transceiver circuits, and produce a very stable reference frequency, i.e., one which is precise and free from fluctuation. Likewise, oscillators compensated for voltage fluctuations and for temperature can also be used to reduce the dependence of the reference frequency on voltage fluctuations and temperature. Furthermore, so-called automatic frequency correction control loops (AFC loops) are frequently used for precisely setting the local reference frequency.

However, it is disadvantageous that these solutions are on the one hand expensive and on the other hand very costly in circuit technology.

In order to keep the costs of a transceiver low, in particular for use in mass produced articles such as mobile telephones, the use presents itself of cheap oscillators which have neither a voltage supply control device nor a temperature control device. However, particularly in such products, no excessive fluctuation of the reference frequency can be tolerated. A subsequent correction of the frequency

of the signals to be processed is therefore unconditionally necessary.

A frequency correction process of a baseband signal x in a transceiver circuit, for example of a mobile radio receiver, can be represented mathematically as follows:

The sampling values x(k) of the baseband signal $x(k) = i(k) + j\,q(k)$ (with $j = \sqrt{-1}$), the symbols of which have a symbol duration T, are multiplied by the sampling values of a (complex) frequency correction signal $z(k) = 2\pi t \cdot T/m\,k$, m being the so-called oversampling factor; this multiplication in the time domain corresponds in the frequency domain to a frequency displacement of the baseband signal x(k) by the frequency f. In the complex signal pointer plane, this represents a rotation of the "pointer" x(k) through the angle z(k):

$$\begin{aligned} x(k)\exp(j\,z(k)) &= [i(k) + j\,q(k)][\cos(z(k)) + j\sin(z(k))] \\ &= [i(k)\cos(z(k)) - q(k)\sin(z(k))] + \\ &\quad j\,[i(k)\sin(z(k)) + q(k)\cos(z(k))] \end{aligned}$$

The more precisely and more finely adjustable the frequency correction signal z(k), the better the frequency correction is effected; i.e., the "pointer" x(k) can be rotated in finer steps in the complex plane.

It would for example to calculate the frequency correction according to the above equation by means of digital multipliers and coefficient tables for the sine and cosine functions; this demands, though, a very high circuit technology cost which makes such a solution expensive and costly. In particular, when embodied as an integrated circuit, this solution requires a large chip surface and is therefore very expensive.

The invention therefore has as its object to provide a process and a circuit arrangement for digital frequency correction, particularly for use in a transceiver

circuit, which produces a very precise frequency correction with a small circuit technology cost.

This object is attained by means of a process with the features of claim 1 and a device with the features of claim 7. Developments of the invention will become apparent from the dependent claims.

A fundamental concept of the invention is to use the CORDIC (Coordinate Rotation Digital Computer) algorithm for the digital frequency correction of a signal. Namely, a frequency and phase correction can be carried out relatively simply by means of the CORDIC algorithm, and the CORDIC algorithm can be carried out with a small circuit technical cost, so that the costs of a circuit based on it -- cheaper oscillator and CORDIC correction -- are smaller than with a costly compensated oscillator.

The CORDIC algorithm is described in J.E. Volder, "The CORDIC trigonometric computing technique", IRE Trans. Electronic Computers, Vol.8, pp. 340-344, 1959; the algorithm is n-fold iterative and serves to rotate a vector through a defined angle $\alpha_n = \arctan(2^{-n})$, $n = 0, 1, ..., N-1$. If the vector represents, as described at the beginning, the pointer of a complex signal, the change of the frequency of the signal corresponding to a multiplication by a frequency correction signal is possible by means of this rotation. The rotation angle becomes smaller with each iteration ($\alpha_0 = 45° > \alpha_1 = 26.6° > ... > \alpha_{N-1}$, so that the frequency of the signal changes in smaller and smaller steps with increasing iteration steps.

The iterative rotation through an angle a can be represented by the following linear combination:

$$a = \sigma_0\alpha_0 + \sigma_1\alpha_1 + ... + \sigma_{N-1}\alpha_{N-1} \qquad (\sigma_n = \pm 1)$$

The precision of the rotation is predetermined by the smallest rotation angle

. α_{N-1}. The direction of rotation (+1 counterclockwise, -1 clockwise) is given by the sign σ_n.

A signal which is represented by sampling values of the in-phase component I_n and the quadrature component Q_n is now iteratively rotated through the angle a by means of the CORDIC algorithm. For this purpose, the individual rotations according to the CORDIC algorithm can be executed by simple shift and addition operations:

$$I_{n+1} = I_n - \sigma_n 2^{-n} Q_n$$
$$Q_{n+1} = \sigma_n 2^{-n} I_n + Q_n$$

The above equation can also be represented as follows, using the equation $\alpha_n = \arctan(2^{-n})$ for the rotation angle:

$$I_{n+1} = \mathrm{sqrt}(1 + 2^{-2n}) [\cos(\sigma_n \alpha_n) I_n - \sin(\sigma_n \alpha_n) Q_n]$$
$$Q_{n+1} = \mathrm{sqrt}(1 + 2^{-2n}) [\sin(\sigma_n \alpha_n) I_n + \cos(\sigma_n \alpha_n) Q_n]$$

After N rotations, there is obtained:

$$I_N = K [\cos(z) I_0 - \sin(z) Q_0]$$
$$Q_N = K [\sin(z) I_0 + \cos(z) Q_0]$$

with K = 1.647. The signal to be corrected can be adjusted in frequency by this means.

In the process according to the invention, the complex multiplication of the sample values x(k) of a signal, particularly of a baseband signal, by a frequency correction signal z(k) is now executed by means of the CORDIC algorithm. Since

there takes place in principle no "rigid" frequency correction, but a frequency correction which is variable because of the CORDIC algorithm, the constancy of the reference signal of an oscillator does not play a large part.

In order to use the CORDIC algorithm for the process according to the invention, a few disadvantages of the CORDIC algorithm must however be compensated for by the invention:

- Since the CORDIC algorithm makes possible only a limited correction range of a rotation angle of approximately 99°, a reduction of the rotation angle required for correction is required. It is provided according to the invention for this purpose to correct the rotation angle so that it always has a value less than or equal to 90°. The rotation angle represented by z(k) is stored modulo 2π in a register of bit width N_w. The value w(k) stored in the register is accumulated according to the equation $w(k) = w(k-1) + f \cdot T/m$. The value 111...111 for w(k) corresponds to the greatest value $1 - 2^{N_w}$, corresponding to an angle of $2\pi(1 - 2^{N_w})$; the modulo 2π operation is thus attained by simply neglecting the overflow of the register.
- Furthermore, it is required for optimum execution of the CORDIC algorithm that the pointer z(k) represented by the frequency correction signal lies in the first or fourth quadrant of the complex I/Q plane. For this purpose, it is provided that the in-phase and quadrature components of the pointer of the signal to be corrected are respectively multiplied by $(-1)^s$, $s = 0.1$, in order then to turn the pointer through the angle $z(k) - \pi$ when the pointer lies in the second or third quadrant of the complex I/Q plane.

The sign flag s is calculated like the sign σ_n for the individual iterations (micro-rotations) of the CORDIC algorithm. According to the invention, a sign table is provided for this purpose, in which the corresponding sign of the

micro-rotation is set out for all possible micro-rotations, such that the sign flag s and the two signs σ_0 and σ_1 are calculated directly and the remaining signs σ_n, n = 2, 3, ..., N-1 are calculated from the bits w_1, w_2, w_3, ..., w_{N+1} of the value w(k) stored in the register.

The bit width N_w of the register and the number of micro-rotations N of the CORDIC algorithm affect the correction range or the phase noise of the frequency-corrected signal x(k) exp(jz(k)) and are therefore to be chosen according to the invention as follows.

The bit width N_w is to fulfill the following inequality for a correctable frequency range Δf:

$$N_w \geq \log2(m) - \log2(\Delta f \cdot T)$$

For a desired signal to phase noise ratio SNR, the number N of the micro-rotations is chosen as follows:

$$(SNR + 3)/6 \leq N \leq N_w - 2$$

The desired signal to phase noise ratio SNR is thus attained, the upper limit for N being predetermined by the bit width of the register.

Finally, another two guard bits have to be provided in each iteration of the algorithm during the implementation of the CORDIC algorithm, in order to be able to process the greatest possible value of the scaling factor, namely sqrt(2) K = sqrt(2) $\cdot$ 1.647 $\approx$ 2.33. K is the scaling factor because of the CORDIC algorithm and sqrt(2) is the possible "growth factor" of the in-phase and quadrature components due to the CORDIC algorithm. Accordingly the input and output bit width of the CORDIC algorithm should be as great as possible, preferably at least greater than N

+ 2. A greater phase noise would otherwise be produced by rounding errors of the CORDIC algorithm than by phase errors.

The following description of preferred embodiments of the invention, using the accompanying drawings, serves for further explanation of the invention.

Fig. 1 shows a block circuit diagram with the essential components for carrying out the process according to the invention,

Fig. 2 shows the structure of a sign table for the CORDIC algorithm,

Fig. 3 shows the structure of a micro-rotation block for the CORDIC algorithm, and

Fig. 4 shows the use of the process according to the invention in a transceiver of a GSM mobile telephone.

In Fig. 1, sampling values i_0 and q_0 of the in-phase or quadrature components of a complex baseband signal x(k) are supplied to a quadrant correction block 10 (k denotes here the discrete sampling times). The quadrant correction block 10 causes the pointer represented by the baseband signal x(k) to lie in the first or fourth quadrant of the complex in-phase/quadrature plane. Namely, if the pointer lies in the second or third quadrant, the CORDIC algorithm does not work correctly. As already described, the in-phase and quadrature components have to be respectively multiplied by -1 if the pointer is situated in the second or third quadrant of the complex I/Q plane.

N micro-rotation blocks in sequence follow the quadrant correction block 10; only three of these blocks, 11, 12, 13, are shown. Each micro-rotation block calculates a step of the CORDIC algorithm, i.e., rotates the pointer represented by the in-phase and quadrature components in the complex I/Q plane through an angle $\pm_n = \pm \arctan(2^{-n})$. The components I_0 and Q_0 are present at the input of the

micro-rotation block 11, and represent at the output, as the components I_1 and Q_1, a pointer rotated through the angle $\pm \alpha_0 = \pm \arctan(1)$. The components I_2 and Q_2 are present at the output of the micro-rotation block 12, and represent a pointer rotated through an angle $\pm \alpha_1 = \pm \arctan((2^{-1}))$. Finally, a pointer represented by the components I_N and Q_N and representing the frequency-corrected complex baseband signal is present at the output of the micro-rotation block 13 after passage through N steps of the CORDIC algorithm. The rotation is either counterclockwise or clockwise in each rotation in a micro-rotation block. The direction of rotation depends on the sign σ_n.

The sign σ_n and the input signal s for the quadrant correction block 10 are produced by the sign table 14. The sign table 14 is driven by a register 31 with a bit width N_w in which a register value w with N_w bits is deposited. The first (N+2) bits of w(k) of the register 31 are supplied to the sign table 14.

The structure of the sign table 14 is shown in Fig. 2. The input signal s for the quadrant block 10 is calculated by a logical XOR operation 16 on the two lowest bits w_0 and w_1 of the register value w. The first sign σ_0 corresponds directly to the bit w_1 of the register value w. The second sign σ_1 is calculated by inverting 17 the bit w_2 of the register value w. The remaining signs σ_2 through σ_{N-1} are deposited in a read-only memory 15 (ROM), in which 2^N (N-2) bits are stored. The ROM or read-only memory 15 can be made smaller by the calculation of s, σ_0 and σ_1 from the three lowest bits w_0-w_2; namely, a memory capacity of 2^{N+2} (N + 1) bits would otherwise be required.

The following table clarifies the calculation of s, σ_0 and σ_1 from the three lowest bits w_0 through w_2 of the register value w, and the corresponding rotation angle range:

w_0	w_1	w_2	Rotation angle range		Quadrant	s	σ_0	σ_1
0	0	0	0°	45°	I	0	0	1
0	0	1	45°	90°	I	0	0	0
0	1	0	90°	135°	II	1	1	1
0	1	1	135°	180°	II	1	1	0
1	0	0	180°	225°	III	1	0	1
1	0	1	225°	270°	III	1	0	0
1	1	0	270°	315°	IV	0	1	1
1	1	1	315°	360°	IV	0	1	0

The signs σ_n are coded such that a logical "0" means a counter-clockwise rotation and a logical "1" means a clockwise rotation.

The input bits of the sign table 14, i.e., of the register value w, are calculated cumulatively, $w(k) = w(k-1) + f \cdot T/m$, starting from the default value $f \cdot T/m$. An adder 18 and a delay element 19 are provided for this purpose. The delay element 18 delays the last register value w(k-1) by the time T/m. The adder then adds the default value $f \cdot T/m$, which predetermines the correction frequency f, to w(k-1). The result of the addition then gives the new register value for the register 31.

The structure of a micro-rotation block, which calculates the basic CORDIC operation described at the beginning,

$$I_{n+1} = I_n - \sigma_n 2^{-n} Q_n$$
$$Q_{n+1} = \sigma_n 2^{-n} I_n + Q_n$$

is shown in Fig. 3. For this purpose, a first and a second shift register, 20 or 21 respectively, are provided, respectively shifting the in-phase component I_n or the

quadrature component Q_n by n bits (2^{-n}). The in-phase component or quadrature component shifted by n bits is then multiplied by the sign σ_n or $-\sigma_n$, i.e., the sign of the displaced component is correspondingly altered, and is added to the original quadrature component Q_n or in-phase component I_n in a first 22 or second 23 accumulator respectively. The result is a rotated pointer, represented by the in-phase component I_{n+1} and the quadrature component Q_{n+1}.

Fig. 4 shows the preferred use of the process according to the invention in a transceiver of a GSM mobile telephone. Sampling values x(k) of a baseband signal are supplied to a digital prefilter 24 which is operated with a high cycle rate, which is a multiple of the sampling rate of 2 of the baseband signal.

Following the digital prefilter 24 is a first decimator 25, which divides the high cycle rate of the output signal of the prefilter 24 into a lower cycle rate.

The first decimator 25 is provided with an offset compensation block 26 for the compensation of a DC offset, i.e., a DC portion, possibly contained in the baseband signal. The offset to be compensated is predetermined for the offset compensation block 26 by a digital signal processor 30. The digital signal processor 30, based on first sampling values of the baseband signal, estimates an offset or DC portion possibly contained in the baseband signal, and supplies this estimated portion to the offset compensation block 26 for compensation. If an offset of the baseband signal were not removed, this offset would be transformed by the CORDIC algorithm into an interfering sine signal, which for example is only to be expensively removed again in the digital signal processor 30.

The offset compensation block 26 is followed by a CORDIC frequency correction block 27 for carrying out the process according to the invention. The correction frequency f by which the baseband signal is to be corrected is supplied to the CORDIC frequency correction block 27 by the digital signal processor 30. The CORDIC frequency correction block 27 corrects the baseband signal frequency, as

previously described, by the correction frequency f.

The CORDIC frequency correction block 27 is followed by a digital postfilter 28, which is cycled at precisely twice the sampling rate 2 of the baseband signal. The digital postfilter 28 is a low pass filter with a very great edge steepness and serves to remove interfering frequencies and noise of the baseband signal.

The frequency-corrected and plurally filtered baseband signal is then decimated by a second decimator 29 by the factor 2 to the sampling rate of the baseband signal, and is supplied to the digital signal processor 30 for further processing.

It should be mentioned here that the process according to the invention and the corresponding device for carrying out the process are also preferred for use for frequency correction in the transmitter and receiver of a UMTS (Universal Mobile Telecommunication System) mobile radio device. A further application is the use of the process according to the invention everywhere in transmitters and receivers where the process according to the invention and the corresponding device serves, in addition to frequency correction, also for digital frequency mixing. Since the functions of frequency correction and frequency mixing are very often used, traditional mixers can be saved in this manner and thus the cost can again be markedly reduced. Examples of such a transmitter and receiver are found in cordless telephones of the DECT standard (Digital Enhanced Cordless Telephone), DVB (Digital Video Broadcasting), and cable modems.

List of Reference Numerals

10	quadrant correction block
11-13	micro-rotation block of the CORDIC algorithm
14	sign table
15	read-only memory (ROM)
16	XOR element
17	inverting
18	adder
19	delay element
20, 21	first, second shift register
22, 23	first, second accumulator
24	digital prefilter
25	first decimator
26	offset compensation block
27	CORDIC frequency correction block
28	digital postfilter
29	second decimator
30	digital signal processor
31	register

PATENT CLAIMS

1. Process for the digital frequency correction of a signal, which is sampled with a sampling cycle (k) and digitalized (x(k), and which is processed by means of an N-step CORDIC algorithm so that the frequency of the signal (x(k)) is altered by a predeterminable frequency, wherein

- the signal (x(k)) is represented by a first vector with the first in-phase component (i_0) and the first quadrature component (q_0) in the complex I/Q plane,
- wherein the first vector is imaged by means of the CORDIC algorithm onto a second vector with a second in-phase component (I_n) and second quadrature component (Q_N), and the second vector represents the signal with an altered frequency and phase,
- wherein the predetermined angle (z(k)) is composed of a plurality of N different rotation angles (α_n),
- wherein each of the different rotation angles (α_n) are calculated according to the formula $\arctan(2^{-n})$, $n = 0, 1, ..., N-1$, and are respectively provided with a sign (σ_n) which gives the direction of rotation.

2. Process according to claim 1, in which the predetermined angle is limited to a range of 0 to 2π in that the angle (z(k)) is represented by a register value (w(k)), the bit width of which prescribes the range of 0-2π for the angle (z(k)), the register value (w(k)) being calculated in each cycle (k) of the sampling cycle by the addition of a value (f·T/m) allocated to the predetermined angle (z(k)) and of the register value w(k-1)) of the preceding cycle (k-1) of the sampling cycle, and an overflow of the register value (w(k)) is neglected.

3. Process according to claim 1 or 2, wherein the predetermined angle (z(k)) is limited to a range of $-\pi/2$ to $+\pi/2$, in that a quadrant correction is carried out before the CORDIC algorithm, whereby the first in-phase component (i_n) and the first quadrature component (q_0) are respectively multiplied by $(-1)^2$, s = 0, 1.

4. Process according to one of the foregoing claims, wherein the bit width N_w of the register value (w(k)) fulfills the following:

$$N_w \geq \log2(m) - \log2(\Delta f \cdot T),$$

where m represents the oversampling factor of the signal (x(k)) and T represents the symbol duration of a digital value of the signal (x(k)).

5. Process according to one of claims 2-4, wherein the number N of the steps of the CORDIC algorithm for a predetermined signal to phase noise ratio SNR and a bit width N_w of the register value (w(k)) fulfills the following condition:

$$(SNR + 3)/6 \leq N \leq N_w - 2.$$

6. Process according to one of the foregoing claims, wherein two guard bits are provided in each step of the CORDIC algorithm, and the input and output bit width of the CORDIC algorithm is at least greater than N + 2.

7. Device for the digital frequency correction of a signal, which is sampled with a sample cycle (k) and is digitized (x(k)),

- in which a series circuit of N micro-rotation blocks (11-13) is provided, to which the signal (i_0, q_0) is supplied,
- a sign (σ_n) is supplied to each micro-rotation block (11-13) from a sign table (14),

- a register (31) is provided, the register value (w(k)) of which is supplied as an address to the sign table (14),
- an adder (18) and a delay element (19) are provided, and the adder (18) adds a predetermined frequency value (f·T/m) to the output value of the delay element (19) and stores the result in the register (31), and the register value of the preceding cycle (k-1) is supplied to the delay element (19).

8. Device according to claim 7, wherein the series circuit of the micro-rotation blocks (11-13) is preceded by a quadrant correction block (10), to which an input signal (s) is supplied, a vector (i_0, q_0) representing the signal being rotated into the first or fourth quadrant of the complex I/Q plane by means of the quadrant correction block (10).

9. Device according to claim 7 or 8, wherein each micro-rotation block (11-13) has two shift registers (20, 21) for shifting the components of an input vector (I_n, Q_n) of the micro-rotation block (11-13) by n bits and two accumulators (22, 23) for adding the components of the input vector (I_n, Q_n) to the output values of the shift registers (20, 21), the output values of the shift registers (20, 21) being provided with the sign (σ_n) allocated to the respective micro-rotation block (11-13).

10. Device according to claim 7, 8 or 9, wherein the sign table (14) has a read-only memory for 2^N (N - 2) bits and an XOR gate (16) and an inverter (17) for the production of the sign (σ_0, σ_1) for the first and second micro-rotation blocks (11, 12) and the input signal (s) for the quadrant correction block (10).

11. Device according to claim 10, wherein the input signal (s) for the quadrant correction block (10) is formed by a logical XOR operation on the two lowest-value bits (w_0, w_1) of the register value (w(k)).

12. Device according to claim 10 or 11, wherein the sign (σ_0) for the first micro-rotation block (11) corresponds to the second bit (w_1) of the register value (w(k)).

13. Device according to claim 10, 11 or 12, wherein the sign (σ_1) for the second micro-rotation block (12) corresponds to the inverted third bit (w_2) of the register value (w(k)).

14. Receiver of a mobile radio device, which has a baseband filter with plural stages (24-30) for filtering and processing a received baseband signal (x(k)), and in which the process according to one of claims 1-6 and/or the device according to one of claims 7-13 is provided before the last stage (28) of the baseband filter for frequency correction of the baseband signal x(k)).

15. Receiver according to claim 14, wherein an offset compensation (26) of the baseband signal (x(k)) is provided for removing DC portions, before the process according to one of claims 1-6 and/or the device according to one of claims 7-13.

16. Receiver according to claim 14 or 15, wherein the receiver is used in a GSM or UMTS mobile radio device.

17 Use of the process according to one of claims 1-6 and/or of the device

according to one of claims 7-13 in a communication system for digital IF mixing and/or frequency correction.

ABSTRACT

The invention relates to a method and a circuit for the digital correction of the frequency of a signal, especially for use in a transmitter/receiver circuit. For the correction of the frequency of a complex digital signal, the signal "pointer" (i_0, q_0) is rotated, by means of the CORDIC algorithm, through a predetermined angle in the complex I/Q plane corresponding to a correction frequency. The CORDIC algorithm has micro-rotation blocks (11-13) corresponding to its N stages, and also a character table (14) and a register (31).

FIG 1

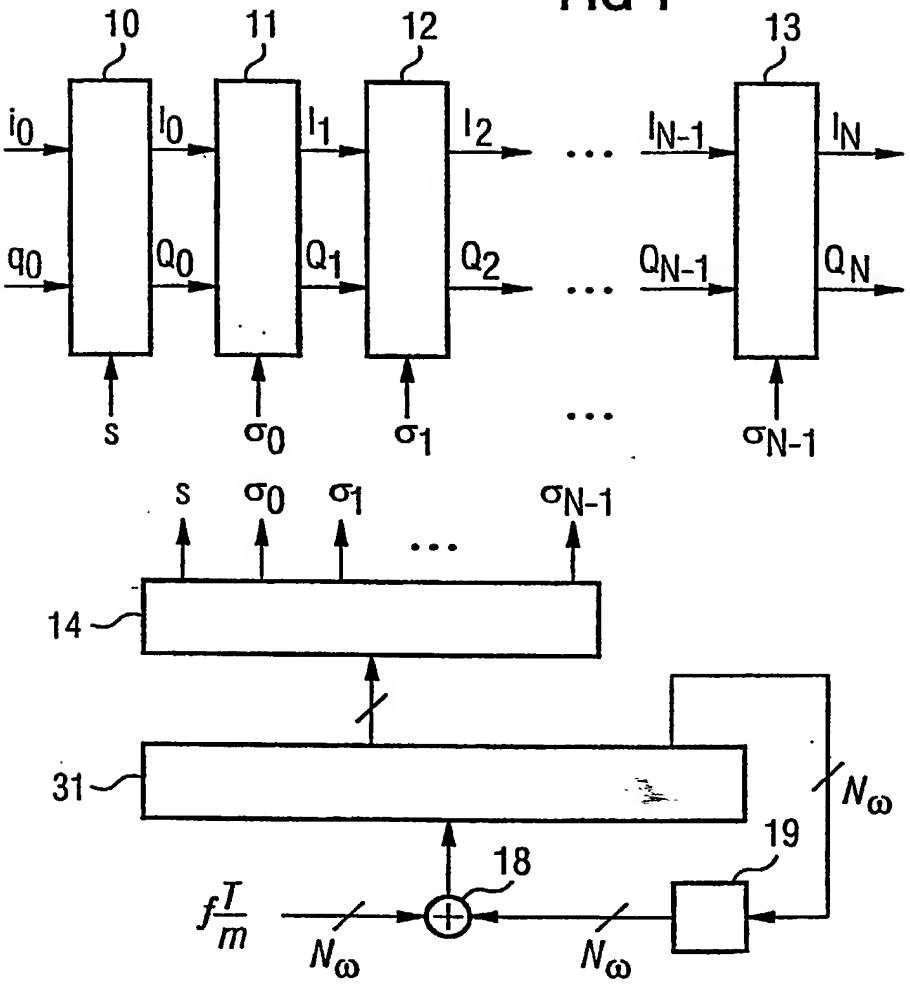
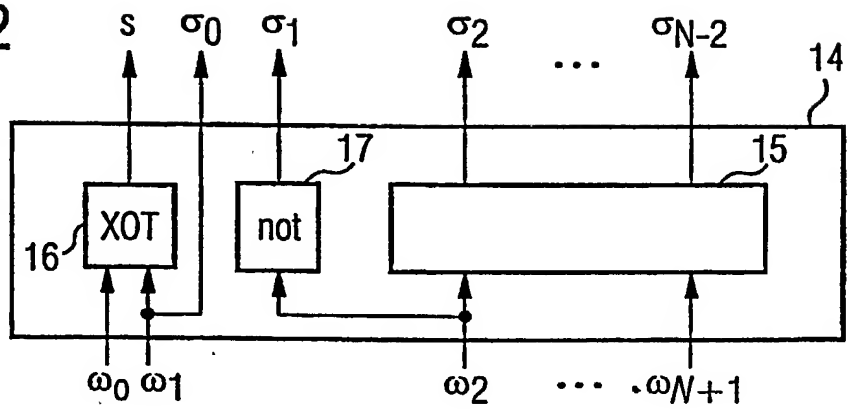

10
11
12
13
i_0
I_0
I_1
I_2
I_{N-1}
I_N
q_0
Q_0
Q_1
Q_2
Q_{N-1}
Q_N
s
σ_0
σ_1
σ_{N-1}
14
31
N_ω
18
19
$f\frac{T}{m}$

FIG 2



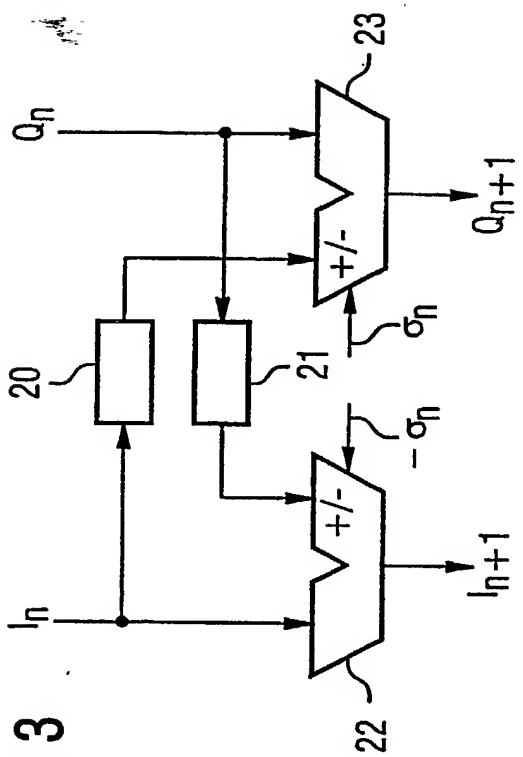


FIG 3

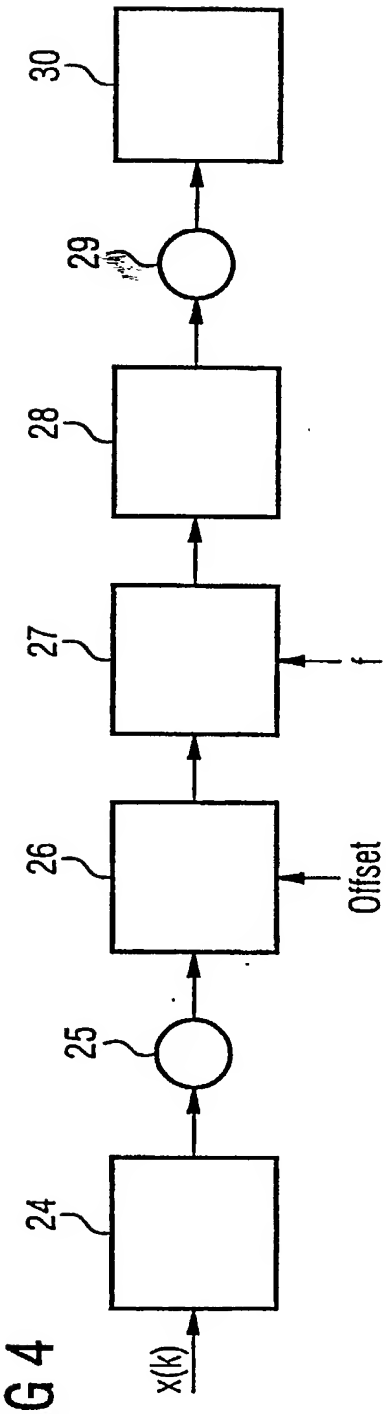


FIG 4

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (Includes Reference to PCT International Applications)	ATTORNEY'S DOCKET NO. 1516.1002

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PROCESS AND CIRCUIT ARRANGEMENT FOR DIGITAL FREQUENCY CORRECTION OF A SIGNAL

the specification of which (check only one item below):

[ ] is attached hereto.

[ ] was filed as United States application
Serial No.
on _____.
and was amended
on _____ (if applicable).

[X] was filed as PCT international application
Number PCT/DE00/03601
on October 11, 2000.
and was amended under PCT Article 19
on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY (if PCT, indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
DE	199 48 899.1	11 October 1999	[X] YES [ ] NO
			[ ] YES [ ] NO
			[ ] YES [ ] NO
			[ ] YES [ ] NO
			[ ] YES [ ] NO

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (Continued) (Includes Reference to PCT International Applications)	ATTORNEY'S DOCKET NO. 1516.1002

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:

U.S. APPLICATIONS		STATUS (Check one)		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED
PCT APPLICATIONS DESIGNATING THE U.S.				
PCT APPLICATION NO.	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED (if any)		
PCT/DE00/03601	11 October 2000		X	

POWER OF ATTORNEY: I hereby appoint the attorneys and agents of Staas & Halsey LLP under USPTO Customer No. 21,171 to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

21171
PATENT TRADEMARK OFFICE

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	POST OFFICE ADDRESS	POST OFFICE ADDRESS c/o Infineon Technologies AG St.-Martin-Straße 53 D-81669 München Bundesrepublik Deutschland	CITY	STATE & ZIP CODE/COUNTRY

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SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
Bin Yang	S. Buch	
DATE 19.6.2002	DATE 17.6.02	DATE